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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/748,359 | 12/30/2003 | Valery M. Dubin | 110348-135103 | 7770 |

31817 7590 10/28/2005

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| EXAMINER | |
|---|---|
| QUACH, TUAN N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/748,359 | DUBIN ET AL. | |
| | Examiner | Art Unit | |
| | Tuan Quach | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/11/2005 has been entered.

### *Rejection 35 U.S.C. 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marathe in view of Aoyama or Chen.

Marathe (6,476,498) teaches regarding claim 1, a semiconductor device comprising a substrate 216, a dielectric layer 212/210 over the substrate, a damascene interconnect structure 232/234/236 defined in the dielectric layer, a barrier layer 232 deposited over the dielectric layer and within the damascene interconnect structure, the barrier layer within the damascene interconnect structure being tapered. See column 6 lines 60-68, Fig. 3. Regarding claim 2, the barrier being thinner toward an edge and thicker toward the bottom is also shown, e.g., portion 231. Regarding claim 3, the via or trench is shown is shown in the openings in dielectric layer. Regarding claim 5, the different barrier materials Thus Marathe lacks anticipation primarily in that it does not recite the damascene interconnect structure having a bottom portion not coupled to a conductive channel.

Aoyama (5,592,024) teaches formation of interconnect wherein a bottom portion can either contact a lower interconnect trench or does not contact a lower interconnect trench. See e.g., Figs. 11G, 13D, 16, 21, 24E, 25E, 26D, 30, 31L, the corresponding descriptions including column 12, lines 46-49 wherein wiring buried in interlayer insulating film 2 is advantageously obtained for a multilayer structure, column 13 line 13-37 wherein a buried wiring is obtained, column 14 line 62, column 17 lines 20-24 wherein a wiring groove can be obtained without connecting to a lower interconnect trench, column 19 lines 65 to form wiring groove 106, column 20 lines 52 et seq. wherein a wiring groove 128 is formed with the a bottom portion not contacting a lower

conductive trench and wiring groove 123 contacting lower conductive trench 124, and column 21 lines 33 et seq. wherein wiring grooves having bottom portion not contacting a conductive trench is also shown.

Chen (6,806,184) teaches opening in dielectric 22 which may an opening created as part of a damascene process and may therefore have the cross section of a singly or a double damascene opening, etched into the surface of the first layer 22 of the dielectric for the creation of an interconnection therein. A single damascene opening comprises an interconnect via or an interconnect trench, a double damascene opening comprises an interconnect via and an interconnect trench. See column 3 lines 34-54.

It would have been obvious to one skilled in the art in practicing Marathe to have employed the damascene structure therein having bottom portions over a conductive trench as well as having bottom portion not contacting a conductive trench, since such would permit the desired conventional structures as shown in Aoyama and Chen and permits contact to the lower trench where desired and permits isolation where contact to a lower trench is not necessary, and such would permit both types of interconnect structures to be obtained using the same layers.

The use of cap layer s well known in the art, e.g., as evidenced by Aoyama, cap 7 over the interconnect for providing protection, see, e.g., column 11 line 20 to column 12 line 22 and such provision to protect the interconnect would have been obvious.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marathe taken with Aoyama or Chen as applied to claims 1-5 and 8 above, and further in view of Farrar.

The references as applied above do not recite all the materials in claim 5, thicknesses in claims 6 and 7, the silicon oxide in claim 8.

Farrar 2002/0024150 teaches the various barrier materials including refractory materials including the selection of appropriate materials, the appropriate thickness for the barrier, and the conventional dielectric such as oxide. See [0051].

It would have been obvious to one skilled in the art to have employed the well known alternative barrier materials, to have selected and optimized the appropriate thickness and to have employed silicon oxide as dielectric material, as claimed in these claims since such correspond to well know materials and dimensions as evidenced by Farrar. Official notice is further given regarding well known alternative barrier materials not expressly recited.

Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marathe taken with Aoyama or Chen (as applied to claims 1-5 and 8 above), and further in view of Farrar and McCown.

The references are applied as above and does not recite the application for connection to microprocessors as in claim 21. Farrar above is applied as above and further teaches conventional application of damascene interconnect for connecting to microprocessors including the bus 452, the microprocessors. See [0066] and Fig. 24.

It would have been obvious to one skilled in the art in practicing the above invention to have applied the interconnect in question into microprocessor interconnection since such is conventional and advantageous applications as evidenced by Farrar. Conversely, it would have been obvious to one skilled in the art to have provided in Farrar the tapered barrer as taught by Marathe to obtain the advantages cited, column 5 lines 53-65, including the provision where a bottom portion not contacting a lower conductive trench if desired or where such contact is unnecessary or necessary as evidenced by Aoyama or Chen. It would have been further obvious to provide the connection to a network interface since such is well known and obvious as evidenced by McCown 2002/0184490, [0025] wherein microprocessor 200B communicates through device bus 202B and network interface 206B. Regarding claim 22-24, these correspond to claims 2-4, respectively, and would have been obvious for the same reasons as delineated above.

Applicant's arguments with respect to claims 1-8 and 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach
Primary Examiner